

BEST AVAILABLE COPY

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10032761	12/27/2001	324	765	2829	Timmy, ✓

**APPLICANTS: Takechi Keizo; Ohsaki Akio; Hayashi Yoshihiko; Murata Kazuhiko;

2829

**CONTINUING DATA VERIFIED:

None

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-150853 05/21/2001

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO
35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		16869N-039000US
Verified and Acknowledged Examiners's initials		
TITLE : Driver circuit integrated with load current output circuit, pin electronics and IC tester having thereof		

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figs. Drwg.
Primary Examiner		Print Fig.	
PREPARED FOR ISSUE		Application Examiner	
DISCLAIMER		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

FILED WITH:

☐ DISK (CRF)

☐ CD-ROM
(Attached in pocket on right inside flap)